Wafer-Scale Patterning of Reduced Graphene Oxide Electrodes by Transfer-and-Reverse Stamping for High Performance OFETs

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A wafer-scale patterning method for solution-processed graphene electrodes, named the transfer-and-reverse stamping method, is universally applicable for fabricating source/drain electrodes of n- and p-type organic field-effect transistors with excellent performance. The patterning method begins with transferring a highly uniform reduced graphene oxide thin film, which is pre-prepared on a glass substrate, onto hydrophobic silanized (rigid/flexible) substrates. Patterns of the as-prepared reduced graphene oxide films are then formed by modulating the surface energy of the films and selectively delaminating the films using an oxygen-plasma-treated elastomeric stamp with patterns. Reduced graphene oxide patterns with various sizes and shapes can be readily formed onto an entire wafer. Also, they can serve as the source/drain electrodes for benchmark n- and p-type organic field-effect transistors with enhanced performance, compared to those using conventional metal electrodes. These results demonstrate the general utility of this technique. Furthermore, this simple, inexpensive, and scalable electrode-patterning technique leads to assembling organic complementary circuits onto a flexible substrate successfully.

1. Introduction

To realize high performance organic field-effect transistors (OFETs) on a flexible substrate, developing good electrode materials and their simple, low-temperature, low-cost, and scalable patterning processes is as critical as researching organic semiconductors. [1–5] Regarding these issues, various solution-processable electrode materials have been investigated. [6–9] For example, numerous research groups demon-
strated OFETs based on poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) electrodes with their electrical performance comparable to those based on common metal electrodes. However, the conductivity of PEDOT:PSS is low and sensitive to moisture, prohibit its practical applications. Dispersions of metal nanoparticles are another candidate for solution-processable electrode materials. However, sintering process, which is necessary to enhance connectivity between the particles and thus the conductivity of the electrode, limits their compatibility with various flexible substrates. Carbon nanotubes (CNTs) or CNT/polymer composite materials have been also utilized as the electrodes for OFETs. However, obtaining bulk quantities of CNTs with suitable purity is challenging and expensive.

More recently, graphene has drawn significant interest as an ideal electrode material for various organic devices due to its low resistivity, high chemical stability, and mechanical strength. Among various types of graphene achievable, the use of solution-processable reduced graphene oxide (rGO) should be the most promising method to exploit graphene electrodes in low cost, large-area, and printed devices on flexible substrates. Accordingly, it is essential to develop versatile methods to pattern rGO electrodes that are electronically compatible (yielding low contact resistance and favorable charge injection) with organic semiconductor layers. Furthermore, the scale-up of these methods should be considered to make significant impact on the field of flexible electronics.

Photolithographic techniques have been applied to create a variety of well-defined rGO patterns by selectively etching unwanted regions of rGO thin films. Such top-down lithographic methods, however, are time-consuming and give rise to undesirable contamination of the patterned rGO surface from contact with photoresist sacrificial layers. As non-lithographic routes for the rGO patterning, micromolding in capillaries, solvent evaporation-driven self-assembly, and various printing techniques including transfer printing, imprinting, and ink-jet printing have also been explored. However, some of these methods are often limited to a simple stripe-type rGO pattern, whereas others are not suitable for the production of high-resolution and reproducible rGO patterns over a large scale.

In this study, we report a wafer-scale patterning of rGO source/drain electrodes that is suitable for forming n- and p-channel OFETs with excellent device performance. This method includes four steps: i) formation of a highly uniform rGO thin film on a glass substrate, ii) transferring of this film onto a hydrophobic silanized substrate, iii) surface energy modulation of both the transferred rGO film and a patterned-elastomeric stamp via oxygen plasma treatment, and iv) selective delamination of the as-treated rGO film using the elastomeric stamp. Based on this method, the size and shape of the rGO patterns with high resolution (<5 μm) could be readily controlled over an entire wafer. These patterns could serve as the source/drain electrodes for benchmark n- and p-channel OFETs based on N,N-diocetyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) and pentacene, respectively. Also, the resulting OFETs exhibited superior device performance, compared to those using conventional metal electrodes, primarily due to enhanced crystallinity of the organic semiconductor layers deposited on top of the rGO electrodes. Furthermore, simple organic complementary circuits (inverters) based on the two n- and p-channel OFETs were successfully assembled onto a flexible substrate. These results demonstrate the general utility of this technique and the excellent compatibility of the as-prepared electrodes with organic semiconductors. We believe that our wafer-scale patterning method of high-resolution rGO microstructures provides a novel approach to realize next-generation organic electronics on plastic substrates.

2. Results and Discussion

Figure 1 and Figure S1 visualize the procedures to prepare rGO source-drain electrodes for bottom-contact/bottom-gate OFETs, which we named as the transfer-and-reverse stamping (TARS) method. TARS method begins with forming a highly uniform and large-area rGO thin film onto a glass (hydrophilic) substrate using the meniscus-dragging deposition (MDD) of graphene oxide (GO) and subsequent chemical reduction process. The as-formed rGO film on the glass substrate is then transferred onto a hexamethyldisilazane (HMDS)-treated Si/SiO2 (hydrophobic) substrate by float-transfer process (the transferring process in TARS method). This transferring step is necessary because highly uniform rGO films cannot be prepared directly on an HMDS-treated hydrophobic substrate due to the hydrophilic nature of GO dispersion. Separately, a polydimethylsiloxane (PDMS) stamp with pre-patterns, which will later define the patterns of rGO, is prepared. Both the rGO films and the PDMS stamp are then treated with oxygen plasma, followed by forming conformal contact between the two treated surface without additional pressurization or heating. The oxygen plasma treatment enabled forming strong adhesion between the two treated-surfaces due to enhanced surface polarity by introducing hydroxyl groups to both surfaces. Because the adhesion between the rGO film and the HMDS-treated SiO2 substrate is relatively weak (See Table S1), rGO film can be selectively delaminated while removing the patterned PDMS stamp (the reverse-stamping process in TARS method). During this reverse-stamping step, the patterns of the PDMS mold should be reversely transferred onto the rGO film.

The key features of TARS method include capability of i) forming rGO patterns based on aqueous dispersion onto a hydrophobic substrate, which is, in general, necessary for achieving high performance OFETs, ii) wafer-scale patterning, as long as one can prepare large PDMS stamp, and iii) obtaining various shaped-and-sized-patterns by designing PDMS stamp delicately. Figure 2a and b display optical micrographs of a transferred rGO film on a 4-inch HMDS-treated SiO2 wafer and the final wafer-scale-patterned rGO electrodes after executing the reverse stamping step, respectively. Figure 2c–h demonstrate the feasibility of TARS method in forming rGO patterns with various shapes, such as spiral squares, zig-zag lines, crosses, circles, squares, and...
Figure 1. Schematic illustration of fabricating rGO source-drain electrodes based on TARS method. (a) Fabrication of GO thin film on a (hydrophilic) glass substrate by the MDD technique, which will be followed by chemical reduction process. (b) Floatation of the rGO thin film. (c) Transfer of the floated rGO thin film onto a HMDS-treated Si/SiO₂ (hydrophobic) substrate. (d) Formation of conformal contact between the rGO film and the pre-patterned PDMS stamp after oxygen plasma exposure to both surfaces. (e) Delamination of the PDMS stamp. (f) Micropatterned rGO electrode arrays. The inset of (f) shows the optical image of the as-patterned rGO electrodes (see also Figure S3a).

Figure 2. Demonstration of wafer-scale micropatterning of rGO thin films. Optical micrographs of (a) rGO thin film and (b) patterned rGO electrode arrays on a 4-in HMDS-treated Si/SiO₂ wafer. The scale bar in an inset of (b) is 1 mm. Optical microscope images of (c) spiral squares, (d) zig-zag lines, (e-h) a variety of arrays (cross, dot, square, and triangle, respectively) on a HMDS-treated Si/SiO₂ substrate.
triangles. In addition, Figure S2 shows that TARS method can form rGO patterns with their resolution below 5 μm.

The as-prepared rGO electrodes were assembled with three different types of organic semiconductors (PTCDI-C8, pentacene, and 6,13-bistrisopropyl-silylthynyl pentacene (TIPS-pentacene)) to examine the general utility of this method for OFET applications. First, PTCDI-C8 semiconductor, a benchmark n-type semiconductor, was thermally deposited onto the channel between the rGO electrodes. Figure 3a shows the output characteristics (drain current ($I_D$) vs. drain voltage ($V_D$)) of a PTCDI-C8 FET with channel length ($L$) of 150 μm and width ($W$) of 800 μm. As expected, typical n-channel behavior, exhibiting a linear regime followed by a saturation regime with increasing $V_D$ under a constant gate voltage ($V_G$) was observed. Under similar operation voltages, the current level of the PTCDI-C8 FETs with rGO electrodes was more than an order of magnitude higher than those using Al electrodes (Figure S4a), which are employed in n-channel OFETs.\[^{46–48}\] More importantly, the PTCDI-C8 FETs with rGO electrodes did not yield super-linear increase in $I_D$ near $V_D = 0$ V (a typical signature of non-ohmic contact as observed from PTCDI-C8 FETs with Al electrodes), indicating good electrical compatibility between PTCDI-C8 and the rGO electrodes.\[^{49}\]

Figures 3b displays transfer characteristics ($I_D$ vs. $V_G$) for PTCDI-C8 FETs with Al, Au, and rGO source-drain electrodes, respectively, at $V_D$ of 60 V. The PTCDI-C8 FETs with rGO electrodes resulted in the most superior device performance compared to others, which demonstrate excellent compatibility of the as-prepared rGO electrodes with PTCDI-C8. First, the ON/OFF current ratio of FETs with the rGO electrodes was more than one order of magnitude higher than that of device with the Al electrodes. Second, the threshold voltage ($V_{th}$) of the device with rGO electrodes was around 1 V, compared to $\sim 23$ V for the Al electrodes. Third, the electron mobility ($\mu$) estimated in the saturation regime ($V_D = 60$ V) using the relationship $I_D = C_i W (V_G - V_{th})^2/(2L)$ (where $C_i$ is the specific capacitance of the gate dielectric (11 nF/cm²))
Table 1. Electrical properties of n-type PTCDI-C8 FETs and p-type pentacene FETs based on various source-drain electrodes.

<table>
<thead>
<tr>
<th>Source-drain electrodes</th>
<th>Carrier mobility [cm²/Vs]</th>
<th>ON/OFF ratio</th>
<th>V GS [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTCDI-C8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rGO</td>
<td>0.39 (±0.13)</td>
<td>4.9 (± 3.1)×10⁷</td>
<td>1.2 (± 3.2)</td>
</tr>
<tr>
<td>Al</td>
<td>0.04 (±0.02)</td>
<td>8.2 (± 5.7)×10⁵</td>
<td>23.4 (± 4.7)</td>
</tr>
<tr>
<td>Au</td>
<td>1.20 (± 0.31)×10⁻⁶</td>
<td>2.4 (± 0.4)×10⁴</td>
<td>28.9 (± 7.9)</td>
</tr>
<tr>
<td>Pentacene</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rGO</td>
<td>0.21 (± 0.09)</td>
<td>7.2 (± 0.9)×10⁴</td>
<td>-3.8 (± 2.8)</td>
</tr>
<tr>
<td>Au</td>
<td>0.04 (± 0.02)</td>
<td>4.1 (± 2.9)×10⁵</td>
<td>-17.4 (± 5.7)</td>
</tr>
<tr>
<td>PEDOT:PSS</td>
<td>0.06 (± 0.02)</td>
<td>1.2 (± 0.9)×10⁴</td>
<td>-10.5 (± 7.4)</td>
</tr>
</tbody>
</table>

was 0.39 cm²/Vs which is around 10 times higher value than that of FETs with Al electrodes (0.04 cm²/Vs). In addition, only weak gate effect was observed from device with Au electrodes, which are commonly used p-channel electrodes, probably due to both high work function of Au (5.01 eV) and poor crystalline nanostructures of PTCDI-C8 on Au electrodes. The summary of the transistor performances, which were obtained from more than 10 devices for each electrodes, are given in Table 1.

In addition, we could estimate contact resistance of the different electrodes. Considering that the total resistance is sum of the contact resistance (independent on V GS) and channel resistance (dependent on V GS),

\[ RW = R_C W + \frac{1}{\mu_C (1/C - R_C W)} \]

should be satisfied in the linear regime, where R is the total resistance and R_C is the contact resistance. Figure 3c shows the width normalized total resistance (RW) of PTCDI-C8 FETs with the rGO and Al contacts under varying V GS and a constant V DS (5 V). For Al electrode devices, RW decreased only up to 15 V, but remained nearly constant above 15 V. The region exhibiting a decrease in RW is where the total resistance is dominated by the channel resistance (the second term in the right-hand side of the equation above) which is inversely proportional to V GS, while the region showing constant RW is where the total resistance is limited by the contact resistance (the first term in the right-hand side of the equation above) which should be independent on V GS. From this plot, the contact resistance could be estimated such that \( R_C W = 9 \times 10^7 \) Ωcm at V GS of 50 V. In contrast, RW for rGO electrode devices decreased gradually with V GS from 0 to 50 V, which indicates that RW is determined predominately by the channel resistance rather than the contact resistance within the given voltage range. Overall, these results demonstrate the improved compatibility of rGO electrodes with PTCDI-C8 compared to that of conventional Al electrodes.

Pentacene, a benchmark p-type organic semiconductor, was also employed to assemble OFETs using the rGO electrodes prepared by TARS method (Figure 3d,e, and Figure S4b). Analogous to the results for PTCDI-C8 OFETs, the rGO electrode devices yielded improved device performance (higher mobility, low threshold voltage, and low contact resistance) than pentacene FETs using conventional p-channel electrode materials, such as Au or PEDOT:PSS.

In addition, we confirmed that the utility of our rGO electrodes can be extended to solution-processable semiconductors such as TIPS-pentacene (Figure S5). Overall, we conclude that the rGO electrodes that were patterned by TARS are applicable to various types of common organic semiconductors and yield superior device performance compared to those based on conventional metal electrodes. The electrical performance of our device is also comparable to those with organic patterned electrodes. To understand the origin of the reduced contact resistance and improved device performance, two factors that can influence the electrode properties are considered. First, the work function of the electrode materials was considered, which is related to the charge injection barrier at the electrode/semiconductor junction. In general, high (low) work function electrode is favorable for hole (electron) injection as thus is suitable for p- (n-) channel OFETs. From ultraviolet photoemission spectroscopy (UPS) measurement, the work function of our rGO electrodes was estimated to be 4.72 eV (Figure S6). This value is higher than that of Al electrodes (4.28 eV) and thus one would expect that electron injection barrier and contact resistance is higher for rGO electrodes than Al electrodes. Analogously, one would expect that hole injection barrier and resulting contact resistance is higher for rGO electrodes than Au electrodes, because the work function for rGO is lower than that of Au (5.01 eV). However, the transistor measurement, as shown above, resulted in the opposite results to the expectation based on work function argument. This implies that work function is not the primary factor determining the improved contact properties of our rGO electrodes.

If not the work function, the other factor of interest is then the surface morphology and the crystal structure of the semiconductor films deposited on electrodes. To address this issue, we characterized PTCDI-C8 and pentacene films deposited on various electrode materials, using AFM and two-dimensional grazing-incidence X-ray diffraction (2D-GIXD). Figure 4a shows AFM images of PTCDI-C8 films deposited onto the rGO and Al electrodes. Two-dimensional PTCDI-C8 grains in layered structure were observed for both films grown on rGO and Al electrodes. The PTCDI-C8 films on rGO exhibited flat terraces and clear step edges separated by monomolecular steps of 2.1 nm, which is in good accordance with previous reports. On the other hand, less ordered crystals with smaller grains were observed from PTCDI-C8 films on Al surface. AFM image of pentacene films deposited on rGO surface (Figure 4b) also showed pronounced morphological differences compared to those on Au. The pentacene films on rGO surfaces exhibited globular structure with average grain size of 165 ± 34 nm, whereas the pentacene films on Au surfaces showed irregularly-shaped grains. The differences in the grain morphologies are probably originated from different surface energy matching and resulting molecular interactions between the semiconductor and electrode surface.
structure of p-type pentacene and n-types PTCDI-C8 films on rGO electrodes was superior compared to those grown on Al and Au surfaces, respectively, which should favorably influence the contact resistance at the electrode/semiconductor junction.

In addition, crystalline structures of PTCDI-C8 and pentacene films deposited on various electrode surfaces were investigated by collecting synchrotron 2D-GIXD measurements (Figure 5). The PTCDI-C8 films deposited on rGO exhibited pronounced Bragg rod reflections up to several orders at various \( q_{xy} \) positions, which indicate the extraordinary crystalline ordering of PTCDI-C8 onto rGO. Meanwhile, the PTCDI-C8 films on Al surface displayed highly scattered intensities for each diffraction peak along the Debye rings, suggesting that the films contain significant crystal mismatch and dislocation in vertical and lateral directions.\(^{[58]}\)

For pentacene films on rGO surfaces, intense \((00l)\) reflection was observed up to fifth order peaks along the \( q_z \) direction, indicating that the pentacene crystals are oriented with their \((00l)\) planes parallel to the substrate surface. Vertically aligned Bragg rod reflections also appeared at various \( q_{xy} \) positions, which are indexed to \( \{1\pm1\}_T, \{0,2\}_T \), and \( \{1,\pm2\}_T \).\(^{[59]}\) This suggests that the pentacene molecules on rGO adopted highly oriented multilayered structure with its \((00l)\) crystal plane directed toward the surface normal. In addition, relatively weak \((001)_b\) peak along the in-plane direction was found, confirming small fraction of lied-down pentacene molecules exist. In contrast, 2D-GIXD for pentacene films on Au contains stronger \((00l)\) peaks along the \( q_{xy} \) axis direction parallel to the substrate, suggesting a flat-lying arrangement of pentacene molecules. Also, highly scattered intensities for each diffraction peak were observed, which should originate...
Wafer-Scale Patterning of Reduced Graphene Oxide Electrodes

from crystal mismatch and dislocations within the film. Overall, these results for both PTCDI-C8 and pentacene films suggest that crystallinity of the films is distinctly improved when the molecules are deposited on rGO electrodes than on common metals. Based on the AFM and x-ray results, therefore, we attribute the reduced contact resistance and enhanced FET performance primarily to the superior film morphology and crystallinity of organic films that were grown on rGO electrodes.

Finally, the rGO electrodes fabricated by TARS were successfully applied to PTCDI-C8 and pentacene FETs and complementary logic circuit (inverter) on a plastic substrate (Figure 6a and Figure S3b). In particular, we utilized poly(ethylene naphthalate) (PEN) substrate coated with indium tin oxide (ITO) gate electrode. Onto these PEN substrates, Al₂O₃ gate dielectric layer (50 nm), rGO electrodes, and semiconductor molecules were successively deposited. Figure 6b and c show typical output and transfer characteristics of the resulting devices, respectively. Note that these devices operated at low voltage below 5 V, due to the use of Al₂O₃ gate dielectric having high specific capacitance. Because our rGO electrodes result in excellent device performance from both PTCDI-C8 and pentacene FETs, a complementary inverter could be readily fabricated by connecting a p-type pentacene FET to an n-type PTCDI-C8 FET. Using a single electrode material for both n- and p-channel while maintaining the good device performance and the resulting capability of forming electrodes for complementary circuits through a single procedure are additional advantages of our method. As shown in Figure 6d, the complementary inverters exhibited good voltage-transfer characteristics. As the supply voltage (V_DD) was increased from 3 to 5 V, the output voltage (V_OUT) remained comparable to the V_DD values at low input voltages (V_IN) and was 0 V at high V_IN. This indicated that the p- and n-type FETs turned on and off, respectively, at low values of V_IN and vice versa at high V_IN. The complementary inverter functioned well over the range of V_DD tested. The signal inverter gain, defined as the absolute value of dV_OUT/dV_IN, is provided in the lower panel of Figure 6d as a function of V_DD. Maximum gain of 15.8 was achieved at V_DD = 5 V.

3. Conclusion

In conclusion, we have developed TARS method which is a highly reproducible and effective method for patterning highly defined, wafer-scale rGO electrode arrays on rigid or flexible hydrophobized substrates for general utility in bottom-contact OFETs. The resulting OFETs (n-type PTCDI-C8 FETs and p-type pentacene FETs) exhibited superior electrical performance (enhanced mobility and reduced contact resistance), compared to devices using common metal electrodes. The improvement was primarily attributed to enhanced crystalline microstructure of semiconductor molecules on rGO compared to those on common metal electrode materials. Furthermore, a transparent and flexible complementary inverter with low voltage operation was successfully demonstrated using the rGO electrodes for p-type and n-type FETs. The novel patterning method or rGO electrodes, which is easy and scalable, offers great promise for next-generation flexible electronics.

4. Experimental Section

Preparation of GO Aqueous Dispersion: GO flakes were prepared from natural graphite powder (Alfa Aesar graphite powder, universal grade, 200 mesh, 99.9999%) by a modified Hummers method[60] and were exfoliated under ultrasonication. The brown dispersion of GO flakes was centrifuged at 8000 rpm for 10 min to remove unexfoliated ones (WiseSpin CF-10, Daihan Scientific) and...
mixed with ultrapure Milli-Q water to obtain GO dispersion with concentration of 2.4 mg/mL.

**Fabrication of PDMS Molds:** Pre-patterned photoresist masters were fabricated by coating SU-8 25 photoresist (MicroChem, Inc.) on a silicon wafer to a thickness of 20 μm using a spin-coater (ACE-200, Spin Coater), and then the wafer was soft-baked. The transparency photomasks containing various pattern printouts were brought into contact with the SU-8 photoresist followed by UV exposure (UV-CURE-60PH, Lichtzen). After a post-baking, the UV-exposed masters were developed in SU-8 developer solution (MicroChem, Inc.) and hard-baked. The PDMS molds for the rGO patterns were created by casting PDMS precursor (Sylgard 184, Dow Corning) on the above SU-8 photoresist masters. After curing the PDMS precursor at 70 °C for 12 h, the mold was peeled off from the master.

**rGO Pattern Formation:** Highly uniform rGO thin films were prepared by forming GO film based on MDD technique and subsequent chemical reduction process. Briefly, two glass slides (one will be used as a coating substrate and the other as a deposition plate (Figure S1)) were hydrophilized with piranha solution for 30 min, thoroughly rinsed with DI water, and dried. A droplet of the GO dispersion with a volume of 16 μL per one centimeter length of deposition plate was injected between the two plates contacting at an angle of 30°. A motorized stage (AL1-1515-3S, Micro Motion Technology) pushed the deposition plate in an alternating motion with a constant linear speed of 20 mm/s to deposit GO sheets on the coating substrate. The resulting GO thin films were chemically reduced by hydriodic (HI) acid vapor at 80 °C for 3 h. The rGO thin films on the glass substrate was then floated on air/water interface (see Figure 1 and Figure S1) and subsequently transferred to HMDS-treated Si/SiO₂ or plastic substrates. The as-prepared rGO film and a separately prepared PDMS molds with patterns were exposed to oxygen plasma (POC-32G, Harrick Plasma) for 30 s at 6.8 W and for 60 s at 18 W, respectively. After forming a stable contact between the two surfaces without additional pressure or heat, the PDMS molds were removed and high-resolution rGO micropatterns were formed.

**Device Fabrication:** OFETs were fabricated using a highly doped n-type Si wafer with a thermally grown 300 nm thick oxide layer as the substrate. The wafer and the oxide layer served as the gate electrode and the gate dielectric, respectively. The wafer was cleaned in a piranha solution for 30 min at 100 °C then washed with copious amounts of distilled water. HMDS (Aldrich Chemical Co.) were treated by a previously reported method. rGO source/drain electrodes were patterned onto the PDMS-treated SiO₂ using TARS method. The channel length and width were 150 and 800 μm, respectively. 50 nm thick pentacene or PTCDI-C8 (Aldrich Chemical Co., no purification) films were deposited from a quartz crucible onto the rGO-patterned substrates at a rate of 0.2 Å/s using a quartz tube reactor (GDM-LX5, Panasonic), an Olympus BX-51 optical microscope, and high-resolution ProRes CF Scan digital CCD camera (Jenoptik). Scanning electron microscopy (SEM) images of the rGO patterns were obtained with a Carl Zeiss SIGMA FE-SEM. The thickness and root-mean-square (rms) roughness of the patterned rGO films were measured using AFM (Digital Instruments Multimode). UPS was performed by a PHI 5000 VersaProbe with a He I (21.2 eV) source. XRD measurements were carried out using the 5A beamline at the Pohang Accelerator Laboratory (PAL), Korea. The pentacene and PTCDI-C8 film morphology was examined by AFM operated in tapping mode. The current–voltage characteristics of the OFETs and inverters were measured at room temperature under vacuum in a dark environment using Keithley 2400 and 236 source/measure units.

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**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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Wafer-Scale Patterning of Reduced Graphene Oxide Electrodes


The work of adhesion \((W_{AD})\) between the layer 1 and 2 is calculated by \(W_{AD} = 4(\gamma_1^p \gamma_2^s(\gamma_1^d + \gamma_2^d) + \gamma_1^s \gamma_2^s(\gamma_1^p + \gamma_2^p))\), where \(\gamma^d\) and \(\gamma^p\) are the dispersion and polar components of overall surface energy of a layer, respectively. Those two contributions to the surface energy were obtained with two testing liquids, water and ethylene glycol, followed by \(\gamma(1 + \cos\theta) = 2(\gamma_1^d \gamma_2^d)^{1/2} + 2(\gamma_1^p \gamma_2^p)^{1/2}\), where \(\gamma\) and \(\theta\) denote the surface energy of a testing liquid and a solid surface, respectively, and \(\theta\) is the contact angle.


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